AMENDMENTS TO SPECIFICATION

Page 1, lines 4-7:

The present invention relates to ~~the~~ a method of fabricating a thin film transistor ~~TFT~~ (TFT) array. It uses the theory of oxidation-reduction to manufacture metal wiring for implementing the metal wiring layout of the TFT-LCDs.

Page 1, lines 10-15:

The quality of ~~the technique is enhancing~~ TFT fabrication increases constantly[[,]]. ~~therefore~~ However, people ~~has~~ make more ~~requirements~~ demands on TFT devices to enhance their life quality. Monochrome display ~~monitor cannot~~ monitors no longer meet ~~for~~ present image industry requirements. Further, the cathode-ray tube CRT has gradually been replaced by the flat panel display FPT as well as the expensive plasma panel display PPD in the color display monitor.

Page 2, lines 16-22:

In order to ~~enhance~~ improve upon the competition for ~~the products in the~~ liquid crystal display ~~LCD~~ (LCD) products, the latest display ~~panel has~~ panels, and in particular the thin-film transistor liquid crystal display (TFT-LCD), have been extensively researched ~~constantly. This may include thin-film transistor liquid crystal display TFT-LCD~~. The conventional TFT-LCD is used in ~~the big-area application~~ large-area applications, and ~~therefore~~ as a result, has the disadvantage of being subject to the delay phenomenon caused ~~from~~ by influence of the resistor capacitor RC ~~influences the result of~~ on the image display.

Page 3, line 23 to Page 4, line 6:

~~More~~ Moreover, the conventional methal wiring process uses an expensive physical vapor deposition method ~~PVD~~ (PVD), and therefore, the manufacturing cost ~~in~~ of the TFT-LCD is more expensive. Apart from this, the consequent thin film process such as etching and high-temperature tempering of the low resistance metal ~~which is with~~ having high diffusion, such as

Cu, ~~has more~~ is troublesome ~~thereto~~ and causes component defects. ~~As a result, the~~ The present invention can overcome the problem of the conventional technique.

Page 2, lines 9-15:

The present invention relates to ~~the~~ a method of fabricating ~~thin film transistor~~ a TFT array. It uses the theory of oxidation reduction to manufacture metal wiring for implementing the metal wiring layout of ~~the~~ TFT-LCDs. ~~More~~ Moreover, it decreases ~~the times of the~~ high-diffusion wiring exposure times in the masking process ~~thereto~~ and decreases ~~the~~ component defects ~~from~~ in the metal wiring ~~while processing in the~~ during multiple masking processes.

Page 2, lines 16-23:

The present invention uses an α-Si [[A-Si]] layer as a seed layer. Then, it uses ~~the~~ a low-resistance metal with stronger oxidation ability for Si as well as ~~uses the~~ a chemical plating method to implement the metal wiring layout of the TFT-LCDs. This, therefore, can replace the lithography etching method ~~being~~ conventionally used in the metal wiring layout ~~as a conventional usage~~. Further, it can enhance the options of the metal wiring material in the TFT-LCD. Besides, the delay phenomena of the resistor capacitor RC can be decreased.

Page 3, lines 6-8:

~~Graphs A-Z of Figure 1~~ Figures 1A -1L ~~is one of the~~ illustrate preferred embodiments according to the present invention by showing the structure of each process in the manufacturing steps; and

Page 3, lines 9-10:

Figure 2 is ~~the circuit diagram using~~ a plan view of a TFT-LCD made by the present invention ~~to make~~.

Page 3, line 13 to Page 4, line 8:

~~Please referring to~~ Figure 1A[[,]] ~~it is~~ illustrates step 1 of one of the preferred embodiments according to the present invention ~~showing step one. First, it uses the~~, in which a mask is used to define the position of the gate electrode metal wiring on the substrate 100. Then, ~~it forms~~ an [[A-Si]] α-Si seed layer 115 is formed on the position. ~~More, the ion of~~ Then, the desired-plated metal 125 and the graphs of the desired-plated area which being are made by ~~stronger~~ relatively strong oxidation-reduction materials processes of ion replacement[[,]] ~~and forms~~ to form the gate electrode 11. The ion of the desired metal can be Cu, Al, Ag, Ni, Ti, W, and Mo. The desired-plated graph ~~of~~ made from the stronger reduction materials can be [[A-Si]] an α-Si seed layer 15. Then, ~~it processes~~ as shown in Fig. 1B, the deposition ~~on~~ of the dielectric layer 205 on the resulting ion-replaced seed layer 116 is carried out, followed by deposition of[[,]] [[A-Si]] α-Si layer 215, and N+ Si layer 225. ~~Please referring to~~ Figure 1B, ~~it is one of the preferred embodiments showing~~ shows step two of the preferred embodiment illustrated in Fig. 1. The [[A-Si]] α-Si layer can ~~use~~ be used as a conducting channel, while the N+ Si layer can ~~use~~ be used as an ~~ohm~~ ohmic contact layer. The above deposition process forming the dielectric layer 205, [[A-Si]] α-Si layer 215, N+ Si layer 225 can use ~~some~~ a variety of deposition methods, which may include[[,]] physical vapor deposition ~~PVD~~, low pressure chemical vapor deposition ~~LPCVD~~, ~~OR~~ or plasma enhanced chemical vapor deposition ~~PECVD~~, ~~and~~ etc. Since oxidation-reduction ion replacement also affects the substrate, substrate 105 is referred-to as substrate 105 in Figs. 1B *et seq.*

Page 4, line 9 to Page 5, line 2:

Following the above step, ~~it~~ the preferred method completes the deposition of the N+ Si layer. Please ~~referring~~ refer to Figure 1C, ~~it is~~ which shows step 3 of the above-described one of the preferred embodiments ~~according to present invention showing step three~~. ~~It~~ This step defines the contact ~~window~~ windows 12[[,]] and shields the partial N+ Si layer 225 against entering the masking process, by using multiple photo-resists 305[[.]] ~~Then, it processes~~ and then using lithography etching for removing ~~un-photo-resist-shielding place thereto forming~~ non-shielded areas to form multiple contact windows 12 between the shielded areas 10, 20, and 30, the non-

etched portions of layers 215 and 225 being indicated by reference numerals 216 and 226. ~~Then, please referring to~~ Figure 1D[[,]] ~~it is one of the preferred embodiments according to the present invention showing~~ shows step 4 of the manufacturing process[[.]] ~~After that, the~~ during which a photo-resist lift-off is ~~processed~~ carried out for implementing the contact window. ~~Please referring~~ refer ~~to~~ Figure 1E[[,]] ~~it is one~~ shows step 5 of the preferred embodiment of the present invention ~~showing step five, and the~~ in which a transparent conducting layer 405 is formed by deposition. The ~~transparent conducting layer 405 can process deposition by the above deposition method. Besides,~~ the material of the transparent conducting layer can be ~~ITO or IZO~~ Indium Tin Oxide (ITO) or Indium-Doped Zinc Oxide (IZO). Then, ~~it defines the~~ a second metal wiring layer is defined on the transparent conducting layer.

Page 5, line 3 to Page 6, line 2:

~~Accordingly, please referring~~ Figure 1F[[,]] ~~it is one~~ step 6 of the preferred ~~embodiments according to the present invention showing step six~~ embodiment. ~~First, it forms the~~ In this step, photo-resist 505[[,]] ~~and defines~~ is used to define the position of the second metal wiring. In the mean time, the source electrode and the drain electrode are defined. Then, ~~it processes the~~ a masking process[[,]] and lithography etching technique are carried out, leaving behind non-etched portions 406 of the transparent conducting layer. The portions of the partial transparent conducting layer ~~is~~ that are removed ~~thereto exposures~~ expose a partial N+ Si layer as a N+ seed layer 407. The N+ Si seed layer [[497]] 407 reacts ~~has the reaction ability~~ with the material of the wiring metal to implement the replacement. The replacement reaction of the wiring metal and the N+ Si seed layer 407 can be ~~the~~ a replacement reaction of same type metals or ~~the~~ an addition reaction. Please ~~referring~~ refer to Figure 1G, ~~it is~~ which shows step 7 of the above-described one of the preferred embodiments according to the present invention ~~showing step seven. It processes~~ This step involves reaction by the chemical electric potential difference of ~~the~~ two substances ~~thereto~~ to form the second metal wiring 408 ~~is formed~~ on the ~~exposure place~~ exposed area of the N+ Si seed layer 407. The ~~place~~ area covered with residue transparent conducting layer cannot have second metal wiring 408 on it, but has a self-alignment. ~~More~~ Moreover, the chemical reaction can use a electrical plating or non-electrical plating method ~~to implement~~. Then, ~~please~~

referring to Figure 1H, ~~it is one of the preferred embodiments according to~~ the ~~present invention showing step eight as well as presenting~~ step 8 is carried out to implement the second metal wiring 408 layout ~~implement~~.

Page 6, lines 3-21:

~~Next step, please referring to~~ Figure [[I]] 1I[[,]] ~~it is one~~ illustrates step 9 of the preferred ~~embodiments according to~~ embodiment of the present invention, ~~showing step nine as well as defining the~~ in which a wiring channel is defined. ~~It uses~~ In this step, photo-resist 605 is used to shield the position of the non-wiring channel. The photo-resist can be a positive-type photo-resist. After ~~entering~~ completing the masking process, ~~the~~ lithography etching is ~~processed~~ used for forming wiring channel 227. Please ~~referring~~ refer to Figure [[I J]] 1J, ~~it is one of the preferred embodiments according to present invention showing ten~~ which shows step 10 of the preferred method. ~~The~~ In this step, wiring channel is implemented and the passivation layer is finally formed ~~finally~~. Please ~~referring~~ refer to Figure 1K, ~~it is one of the preferred embodiments according to the present invention showing~~ which shows step eleven. By using the above deposition method, ~~it deposits~~ a passivation layer is deposited, and then the fourth photo-resist 710 is placed on the component. ~~More~~ Moreover, the passivation layer 700 without the fourth photo-resist covering is removed for forming the component passivation layer 706. Further, the fourth photo-resist 710 is removed. ~~Please referring to~~ In step 11 shown in Figure 1L, ~~it is one of the preferred embodiments according to present invention showing twelve as well as showing the~~ manufacture of the TFT array is completed.

Page 6, line 22 to Page 7, line 18:

Please ~~referring~~ refer to Figure 2, ~~it is the circuit diagram using~~ which shows a circuit made by the present invention ~~to make~~. ~~From description of the circuit diagram~~ According to the above description, the first masking process is processed firstly for forming the first metal wiring 11. Also, ~~it~~ the first masking process defines the position of the gate electrode. The wiring metal of the gate electrode is ~~used~~ implemented by means of the replacement method ~~to implement~~. Then, ~~it uses the definition of the~~ a second masking process is used to form a signal

area and the contact window ~~thereto deposit~~ by depositing the transparent conducting layer 14. Further, the third masking process ~~is processed to define~~ defines the source electrode and the drain electrode 13. The wiring metal can be a partial N+ Si layer in order to process the self-alignment replacement reaction for the seed. ~~More~~ Moreover, ~~the~~ a fourth masking process is ~~processed~~ carried out for forming a wiring channel 17. Then, the fifth masking process is used as the process for forming a passivation layer 15. The method of fabricating ~~thin film transistor~~ a TFT according to the present invention ~~more~~ focuses more on the gate ~~in~~ during initial ~~forming status~~ formation, and on the third masking process. It uses the oxidation-reduction character of the chemical plating method to form ~~a~~ metal wiring for implementing the metal wiring layout of the TFT-LCDs. Further, it can avoid the exposure of the metal wiring ~~happening in~~ that occurs during the masking process, ~~as well as the~~ and thereby prevent component ~~defect~~ defects from occurring.

Page 7, lines 19-23:

Please cancel this paragraph in its entirety, beginning with "In conclusion, the..." and ending with "can be granted as a patent."